CURRICULUM VITAE

Alvin R. Lebeck

June 22, 2017

Department of Computer Science
D308 Levine Science Research Center
Box 90129
Duke University
Durham, NC 27708-0129

E-mail: *alvy@cs.duke.edu*
Office phone: (919) 660-6551
Department phone: (919) 660-6500
Fax: (919) 660-6519
URL: *http://www.cs.duke.edu/~alvy*

Employment History:

1. **Professor**, Department of Computer Science, Duke University, 2007—present.
2. **Co-Founder,** PHITONEX, INC. June 2017.
3. **Consulting Researcher**, Microsoft Research, Jan 2013—June 2017.
4. **Visiting Researcher**, eXtreme Computing Group, Microsoft Research, Jul—Dec 2012.
5. **Associate Professor**, Department of Computer Science, Duke University, 2003—2007.
6. **Assistant Professor**, Department of Computer Science, Duke University, 1996—2002.

Education:

1. **Ph.D. in Computer** Science, University of Wisconsin at Madison, November 1995.
   Advisor: Professor David A. Wood.
   Thesis: Tools and Techniques for Memory System Design and Analysis.
2. **Master of Science** in Computer Science, University of Wisconsin at Madison, December 1991.
   Advisor: Professor Gurindar S. Sohi.
   Thesis: Request Combining in Multiprocessors with Arbitrary Interconnection Networks.
3. **Bachelor of Science** in Electrical and Computer Engineering (Dean's honor list), University of Wisconsin at Madison, May 1989.

Honors and Awards:

1. IEEE Fellow class of 2017.
2. Best paper awards
   a. 31st Annual ACM/IEEE International Symposium on Microarchitecture, November 1998.
   b. 6th International Workshop on Network on Chip Architectures, December 2013.
3. IEEE Top Picks from Computer Architecture Conferences in 2009, 2010, 2017 (honorable mention).

4. NSF CAREER Award 1997.
5. Outstanding Graduate Student Researcher, Department of Computer Sciences, University of Wisconsin—Madison, 1995.

Journal Publications:

1. Craig LaBoda, Chris Dwyer, Alvin R. Lebeck, "Exploiting Dark Fluorophore States to Implement Resonance Energy Transfer Pre-Charge Logic", to appear in IEEE MICRO Special Issue on Post-Moore Computing, July/August 2017.
2. Craig LaBoda, Alvin R. Lebeck, Chris Dwyer , "An Optically Modulated Self-Assembled Resonance Energy Transfer Pass Gate", Nano Letters, ACS Publications, Nano Letters, 17(6), pp 3775-3781, 2017.
3. S. Yang, A. R. Lebeck, C. Dwyer, "Nanoscale Resonance Energy Transfer-based Devices for Probabilistic Computing," in *IEEE Micro*, Volume 35, Issue 5, pages 72-84, September/October 2015.
4. J. Pang, C. Dwyer, A. R. Lebeck, "mNoC: Large Nanophotonic Network-on-Chip Crossbars with Molecular Scale Devices," in *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Volume 12, Issue 1, pages 1-25, July 2015.
5. J. Pang, C. Dwyer, A. R. Lebeck, "Modeling and Simulation of a Nanoscale Optical Computing System," *Journal of Parallel and Distributed Computing Special Issue on Nanoarchitectures*, Volume 74, Issue 6, pages 2470-2483, June 2014, available online August 2013.
6. B. F. Romanescu, Alvin R. Lebeck, and Daniel J. Sorin, "Address Translation-Aware Memory Consistency," in *IEEE Micro Top Picks from Computer Architecture Conferences of 2010*, Volume 31, Issue 1, pages 109-118, January/February 2011.
7. M. Zhang, A. R. Lebeck, D. Sorin, "Fractal Consistency: Architecting the Memory System to Facilitate Verification", *IEEE Computer Architecture Letters*, Volume 9, Issue 2, pages 61-64, November 2010.
8. C. Pistol, V. Mao, A. R. Lebeck, C. Dwyer, "Encoded Multi-Chromophore Response for Simultaneous Label-Free Detection," in Small, Volume 6, No. 7, pages 843-850, April 9 2010.
9. Y. Liu, C. Dwyer, A. R. Lebeck, "Routing in Self-organizing Nano-scale Irregular Networks," in *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Volume 6 , Issue 1, pages 1-21, March 2010.
10. C. Pistol, W. Chongchitmate, C. Dwyer, and A. R. Lebeck, "Architectural Implications of Nano-scale Integrated Sensing and Computing," in *IEEE Micro Top Picks from Computer Architecture Conferences of 2009,* 30(1), pages 110-120, January/February 2010.
11. C. Pistol, C. Dwyer, A. R. Lebeck, "Nanoscale Optical Computing using Resonance Energy Transfer Logic," in *IEEE Micro*, 28 (6), pages 7-19 November/December 2008.
12. J. P. Patwardhan, C. Dwyer, A. R. Lebeck, "A Defect Tolerant Self-organizing Nanoscale SIMD Architecture," in *ACM Journal on Emerging Technologies in Computing Systems (JETC), 3(2), July* 2007.

13. T. Li, A. R. Lebeck, D. J. Sorin, "Spin Detection Hardware for Improved Management of Multithreaded Systems," in *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, 17(6), pages 508-521, June 2006.

14. J. Patwardhan, C. Dwyer, A. R. Lebeck, D. J. Sorin, "NANA: A Nanoscale Active Network Architecture," in *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, 2 (1), pages 1-30, January 2006.

15. S. H. Park, C. Pistol, S. J. Ahn, J. H. Reif, A. R. Lebeck, C. Dwyer, T. H. LaBean, "Finite-size, Fully-Addressable DNA Tile Lattices Formed by Hierarchical Assembly Procedures," in *Angewandte Chemie*, 45(5), pages 735-739, January 23, 2006.

16. H. Zeng, C. S. Ellis, A. R. Lebeck, "Experiences in Managing Energy with ECOSystem," in *IEEE Pervasive Computing*, 4 (1), pages 62-68, January 2005.

17. C. Dwyer, A. R. Lebeck, D.J. Sorin, "Self-assembled Architecture and the Temporal Aspects of Computing", in *IEEE Computer*, 38 (1), pages 56-64, January 2005.

18. C. Yang, A. R. Lebeck, Hung-Wei Tseng, Chien-Hao Lee "The Push Architecture: a Prefetching Framework for Linked Data Structures," in *ACM Transactions on Architecture and Code Optimization (ACM TACO)*, 1(4), pages 445 - 475, December 2004.

19. C. Dwyer, V. Johri, J. P. Patwardhan, A. R. Lebeck, and D. J. Sorin, "Design Tools for Self-assembling Nanoscale Technology," in *Institute of Physics Nanotechnology,* 15 (9) pages 1240-1245, September 2004.

20. M. Thottethodi, A. R. Lebeck, S. Mukherjee, "Exploiting Global Knowledge to Achieve Self-Tuned Congestion Control for k-ary n-cube Networks," in *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, 15 (3), pages 257-272, March 2004.

21. S. Chatterjee, A. R. Lebeck, Praveen K. Patnala, M. Thottethodi, "Recursive Array Layouts and Fast Parallel Matrix Multiplication," in *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, 13(11), pages 1105-1123, November 2002.

22. P. J. Hanlon, D. Chung, S. Chatterjee, D. Genius, A. R. Lebeck, and E. Parker, "The Combinatorics of Cache Misses During Matrix Multiplication", in *Journal of Computer Sciences and Systems,* 63(1). pages 80-126, August 2001.

23. C. Yang, B. Sano, and A. R. Lebeck, "Exploiting Parallelism in Geometry Processing with General Purpose Processors and Floating-Point SIMD Instructions", In *IEEE Transactions on Computers*, 49(9), pages 934-946, September 2000.

24. S. T. Srinivasan and A. R. Lebeck, "Load Latency Tolerance in Dynamically Scheduled Processors", In the *Journal on Instruction-Level Parallelism*, vol. 1, November 1999 (http://www.jilp.org/vol1). (**Invited Paper**)

25. A. R. Lebeck and D. A. Wood, "Active Memory: A New Abstraction for Memory System Simulation," In *ACM Transactions on Modeling and Computer Simulation (ACM TOMACS)*, 7(1), pages 42-77, January 1997.

26. A. R. Lebeck and D. A. Wood. "Cache Profiling and the SPEC Benchmarks: A Case Study," *IEEE Computer*, 27(10), pages 15–26, October 1994.

27. A. R. Lebeck and G. S. Sohi. "Request Combining in Multiprocessors with Arbitrary Interconnection Networks," *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, 5(11), pages 1140-1155, November 1994.

28. D. A. Wood, S. Chandra, B. Falsafi, M. D. Hill, J. R. Larus, A. R. Lebeck, J. C. Lewis, S. S. Mukherjee, S. Palacharla, and S. K. Reinhardt. "Mechanisms for Cooperative Shared Memory". In *CMG Transactions*, Issue 84, Spring 1994, pages 51-62.

Books:

29. C. Dwyer and A. R. Lebeck, "Introduction to DNA Self-Assembled Computer Design", ISBN-13 978-1596931688, Artech House Publishers, January 2008.

Book Contributions:

30. C. Dwyer and A. R. Lebeck, "Self-Assembled Computer Architecture". Systems Self-Assembly: Multidisciplinary Snapshots, Natalio Krasnogor, Steve Gustafson, David Pelta and Jose L. Verdegay (Eds.), ISBN-13: 978-0-444-52865-0, Elsevier, 2008.

31. I. Schoinas, B. Falsafi, A. R. Lebeck, S. K. Reinhardt, J. R. Larus, and D. A. Wood. "Fine-Grain Access Control for Distributed Shared Memory". Distributed Shared Memory: Concepts and Systems, by Jelica Protic, Milo Tomaevic and Veljko Milutinovic, ISBN 0-8186-7737-6, IEEE Computer Society Press, 1997.

Refereed Conference and Symposia Publications:

32. Pulkit Misra, Jeffrey S. Chase, Johannes Gehrke, Alvin R. Lebeck, "Enabling Lightweight Transactions with Precision Time," in *Proceedings of the Twenty Second International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS),* April 2017. To appear.

33. Siyang Wang, Xiangyu Zhang, Yuxuan Li, Ramin Bashizade, Song Yang, Chris Dwyer, Alvin R. Lebeck, "Accelerating Markov Random Field Inference using Molecular Optical Gibbs Sampling Units," in *Proceedings of the 43rd International Symposium on Computer Architecture (ISCA)*, pages 558-569, June 2016. (**Also IEEE Top Picks '17 Honorable Mention**).

34. S. R. Agrawal, C. M. Dee, A. R. Lebeck, "Exploiting Accelerators for Efficient High Dimensional," in *Proceedings of the 21st ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP '16),* March 2016.

35. J. Pang, C. Dwyer, A. R. Lebeck, "More is Less, Less is More: Molecular-Scale Photonic NoC Power Topologies," in *Proceedings of the Twentieth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS),* pages 283-296, March 2015.

36. S. R. Agrawal, V. Pistol, J. Pang, J. Tran, D. Tarjan, A. R. Lebeck, "Rhythm: Harnessing Data Parallel Hardware for Server Workloads," in *Proceedings of the Nineteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS),* pages 19-34, March 2014.

37. Meng Zhang, Alvin R. Lebeck, Daniel J. Sorin, "Fractal Coherence: Scalably Verifiable Cache Coherence," in *Proceedings of the 43rd Annual IEEE/ACM International Symposium on Microarchitecture, 2010 (MICRO 2010)*, pages 471-482, December 2010.

38. Bogdan F. Romanescu, Alvin R. Lebeck, and Daniel J. Sorin, "Specifying and Dynamically Verifying Address Translation-Aware Memory Consistency," in *Proceedings of the Fifteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '10)*, pages 323-334, March 2010.

39. Bogdan F. Romanescu, Alvin R. Lebeck, Daniel J. Sorin, and Anne Bracy. "UNified Instruction/Translation/Data (UNITD) Coherence: One Protocol to Rule Them All," in *16th IEEE International Symposium on High-Performance Computer Architecture*, January 2010.

40. C. Pistol, W. Chongchitmate, C. Dwyer, and A. R. Lebeck, "Architectural Implications of Nano-scale Integrated Sensing and Computing," in *Proceedings of the Fourteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '09)*, pages 13-24,March 2009.

41. A. R. Lebeck, C. Dwyer, "Self-Organizing Defect Tolerant, Self-Assembled Nanoscale Architectures," in *Nanoelectronic Devices for Defense and Security Conference*, June 2007.

42. J. Patwardhan, V. Johri, C. Dwyer, A. R. Lebeck, "A Defect Tolerant Self-organizing Nanoscale SIMD Architecture," in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XII)*, pages 241-251, October 2006. (25% acceptance rate).

43. J. Patwardhan, C. Dwyer, A. R. Lebeck, "Self-Assembled Networks: Control vs. Complexity," *1st International Conference on Nano-Networks (NANONETS)*, September 2006

44. C. Pistol, C. Dwyer, A. R. Lebeck, "Design Automation for DNA Self-Assembled Nanostructures," in *Proceedings of the 43rd Design Automation Conference (DAC)*, July, 2006. (18% acceptance rate).

45. T. Li C. S. Ellis, A. R. Lebeck, D. J. Sorin, "Pulse: A Dynamic Deadlock Detection Mechanism using Speculative Execution," in *Proceedings of USENIX Annual Technical Conference*, April 2005. (20% acceptance rate.)

46. J. P. Patwardhan, C. Dwyer, A. R. Lebeck, D. J. Sorin, "Circuit and System Architecture for DNA-Guided Self-Assembly of Nanoelectronics," in *Proceedings of the Foundations of Nanoscience: Self-Assembled Architectures and Devices (FNANO)*, April 2004. (**Invited Paper**)

47. J. Patwardhan, A. R. Lebeck, D. J. Sorin, "Communication Breakdown: Analyzing CPU usage in Commercial Web Workloads," in *International Symposium on Performance Analysis of Systems and Software (ISPASS '04)*, March 2004.

48. T. Li, A. R. Lebeck, D. J. Sorin, "Quantifying Instruction Criticality for Shared Memory Multiprocessors," in *Proceedings of the International Symposium on Parallelism in Algorithms and Architectures (SPAA)*, June 2003.

49. H. Zeng, C. S. Ellis, A. R. Lebeck, A. Vahdat, "Currentcy: A Unifying Abstraction for Expressing Energy Management Policies," in *Proceedings of USENIX Annual Technical Conference*, June 2003.

50. M. Thottethodi, A. R. Lebeck, S. Mukherjee, "BLAM : A High-Performance Routing Algorithm for Virtual Cut-Through Networks," in *Proceedings of the International Parallel and Distributed Processing Symposium (IPDPS)*, April 2003. (30% acceptance rate)

51. H. Zengh, C. S. Ellis, A. R. Lebeck, A. Vahdat, "ECOSystem: Managing Energy as a First Class Operating System Resource," in Proceedings of the Tenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS X), pages 123-132, October 2002. (18% acceptance rate)

52. A. R. Lebeck, J. Koppanalil, T. Li, J. Patwardhan, E. Rotenberg, "A Large, Fast Instruction Window for Tolerating Cache Misses," in *Proceedings of the 29th International Symposium on Computer Architecture (ISCA)*, pages 59-70, May 2002. (15% acceptance rate)

53. C. Yang and A. R. Lebeck, "A Programmable Memory Hierarchy for Prefetching Linked Data Structures," in *Proceedings of the 4th International Symposium on High Performance Computing*

(ISHPC-IV), G. Goos, J. Hartmanis, and J. van Leeuwen Eds. Springer Lecture Notes in Computer Science, vol. 2327, May 2002.

54. X. Fan, C. S. Ellis, A. R. Lebeck, "Memory Controller Policies for DRAM Power Management," in *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*, pages 129-134, August, 2001. (13% acceptance rate)

55. S. T. Srinivasan, C. Wilkerson, R. Ju, and A. R. Lebeck, "Locality vs. Criticality," in *Proceedings of the 28th International Symposium on Computer Architecture (ISCA)*, pages 132-143, June 2001. (15% acceptance rate)

56. S. Chatterjee, E. Parker, P. Hanlon, A. R. Lebeck, "Exact Analysis of the Cache Behavior of Nested Loops," in *Proceedings of the International Symposium on Programming Language Design and Implementation (PLDI)*, pages 286-297, June 2001. (20% acceptance rate)

57. M. Thottethodi, A. R. Lebeck, S. Mukherjee, "Self-tuned Congestion Control for Multiprocessor Networks," in *Proceedings of the Seventh International Symposium on High Performance Computer Architecture (HPCA-7)*, pages 107-118, January 2001. (23% acceptance rate)

58. A. R. Lebeck, X. Fan, H. Zengh, C. S. Ellis, "Power Aware Page Allocation," in Proceedings of the Ninth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS IX), pages 105-116, November 2000. (21% acceptance rate)

59. A. Vahdat, A. R. Lebeck, C. S. Ellis, "Every Joule is Precious: The Case for Revisiting Operating System Design for Energy Efficiency," in *ACM SIGOPS European Workshop*, September 2000.

60. C. Yang and A. R. Lebeck, "Push vs. Pull: Data Movement for Linked Data Structures," in *Proceedings of the 14th ACM International Conference on Supercomputing,* pages 176-186, May 2000. (26% acceptance rate)

61. J. S. Chase, D. C. Anderson, A. J. Gallatin, A. R. Lebeck, and K. G. Yocum, "Network I/O with Trapeze," in *IEEE Hot Interconnects*, August 1999. (**Invited Paper**)

62. A. R. Lebeck, D. R. Raymond, M. S. Thottethodi, and C. Yang, "Annotated Memory References: A Mechanism for Informed Cache Management," in *Proceedings of the 5th International Euro-Par Conference*, Lecture Notes in Computer Science 1685, P. Amestoy et al. (Editors), Springer-Verlag, pages 1251-1254, August 1999. (54% acceptance rate)

63. S. Chatterjee, A. R. Lebeck, Praveen K. Patnala, M. Thottethodi, "Recursive Array Layouts and Fast Parallel Matrix Multiplication," in *Proceedings of the 11th ACM Symposium on Parallel Algorithms and Architectures (SPAA)*, pages 222-231, June 1999. (29% acceptance rate)

64. S. Chatterjee, V. Jain, A. R. Lebeck, S. Mundhra, M. Thottethodi, "Nonlinear Array Layouts for Hierarchical Memory Systems," in *Proceedings of the 13th ACM International Conference on Supercomputing*, pages 444-453, June 1999. (28% acceptance rate)

65. A. R. Lebeck, "Cache Conscious Programming in Undergraduate Computer Science," in *Proceedings of the 30th SIGCSE Technical Symposium on Computer Science Education*, pages 247-251, March 1999. (39% acceptance rate)

66. S. T. Srinivasan and A. R. Lebeck, " Load Latency Tolerance in Dynamically Scheduled Processors," in *Proceedings of the 31st Annual International Symposium on Microarchitecture (MICRO)*, pages 148-159, November 1998. (**Best paper award**, 26% acceptance rate)

67. C. Yang, B. Sano, and A. R. Lebeck, "Exploiting Instruction Level Parallelism in Geometry Processing for Three Dimensional Graphics Applications," in *Proceedings of the 31st Annual*

International Symposium on Microarchitecture (MICRO), pages 14-24, November 1998. (26% acceptance rate)

68. M. S. Thottethodi, S. Chatterjee, and A. R. Lebeck, "Tuning Strassen's Matrix Multiplication for Memory Efficiency," in *Proceedings of Supercomputing 98*, November 1998. (Best student paper finalist, 25% acceptance rate)

69. V. P. Pauca, X. Sun, S. Chatterjee, and A. R. Lebeck, "Architecture-Efficient Strassen's Matrix Multiplication: A Case Study of Divide-and-Conquer Algorithms," in *International Linear Algebra Society (ILAS) Symposium on Algorithms for Control, Singles, and Image Processing*, June 1997.

70. K. Yocum, J. Chase, A. Gallatin, and A. R. Lebeck, "Cut-Through Delivery in Trapeze: An Exercise in Low-Latency Messaging," in *Proceedings of the IEEE International Conference on High Performance Distributed Computing (HPDC)* August 1997. (47% acceptance rate)

71. A. R. Lebeck and D. A. Wood, "Dynamic Self-Invalidation: Reducing Coherence Overhead in Shared- Memory Multiprocessors," in *Proceedings of the 22nd Annual International Symposium on Computer Architecture (ISCA)*, pages 48-59, June 1995. (20.5% acceptance rate)

72. A. R. Lebeck and D. A. Wood, "Active Memory: A New Abstraction for Memory System Simulation," in *Proceedings of the 1995 ACM Sigmetrics Conference on Measurement and Modeling of Computer Systems,* pages 220-230, May 1995. (21.9% acceptance rate)

73. I. Schoinas, B. Falsafi, A. R. Lebeck, S. K. Reinhardt, J. R. Larus, and D. A. Wood, "Fine-Grain Access Control for Distributed Shared Memory," in *Proceedings of the Sixth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-VI)*, pages 297-306, October 1994. (19.9% acceptance rate)

74. B. Falsafi, A. R. Lebeck, S. K. Reinhardt, I. Schoinas, M. D. Hill, J. R. Larus, A. Rogers, and D. A. Wood, "Application-Specific Protocols for User-Level Shared Memory," in *Proceedings of Supercomputing 94*, pages 380-389, November 1994.

75. S. K. Reinhardt, M. D. Hill, J. R. Larus, A. R. Lebeck, J. C. Lewis, and D. A. Wood, "The Wisconsin Wind Tunnel: Virtual Prototyping of Parallel Computers," in *Proceedings of the 1993 ACM Sigmetrics Conference on Measurement and Modeling of Computer Systems*, pages 48–60, May 1993.

76. D. A. Wood, S. Chandra, B. Falsafi, M. D. Hill, J. R. Larus, A. R. Lebeck, J. C. Lewis, S. S. Mukherjee, S. Palacharla, and S. K. Reinhardt, "Mechanisms for Cooperative Shared Memory," in *Proceedings of the 20th Annual International Symposium on Computer Architecture (ISCA),* pages 156–167, May 1993. (15.7% acceptance rate)

77. R. E. Kessler, R. J. Jooss, A. R. Lebeck, and M. D. Hill, "Inexpensive Implementations of Set-Associativity," in *Proceedings of the 16th Annual International Symposium on Computer Architecture (ISCA)*, pages 131–139, June 1989. (27% acceptance rate)

Refereed Workshop Publications:

78. J. Pang, C. Dwyer A. R. Lebeck, "Exploiting Emerging Technologies for Nanoscale Photonic Networks-on-Chip," in *Sixth International Workshop on Network on Chip Architectures (NoCArc-13)*, December 2013. **Best Paper Award**

79. Y. Liu, A. R. Lebeck, "Nano-scale On-chip Irregular Network Analysis," *Proceedings of ICCCN 09 Workshop on Nano Molecular and Quantum Information Networks (NanoCom)*, August 2009.

80. C. Dwyer, A. R. Lebeck, C. Pistol, "Energy Transfer Logic on DNA Nanostructures: Enabling Molecular-Scale Amorphous Computing," in *Proceedings of the 4th Workshop on Non-Silicon Computing*, pages 33-40, June 2007.

81. A. R. Lebeck, and C. Dwyer, "Self-Organizing, Defect Tolerant, Self-Assembled Nanoscale Architectures," in *Nanoelectronic Devices for Defense and Security*, June 2007.

82. J. Patwardhan, C. Dwyer, A. R. Lebeck, "Design and Evaluation of Fail-Stop Self-Assembled Nanoscale Processing Elements," in *IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH '06)*, June 2006.

83. Jaidev P. Patwardhan, Chris Dwyer, Alvin R. Lebeck, Daniel J. Sorin, "Evaluating the Connectivity of Self-Assembled Networks of Nano-scale Processing Elements," in *IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH '05)*, May 2005.

84. X. Fan, C. S. Ellis, A. R. Lebeck, "The Synergy between Power-aware Memory Systems and Processor Voltage Scaling," in *Proceedings of the Workshop on Power Aware Computing Systems 2003 (PACS '03)*, Springer-Verlag Lecture Notes in Computer Science, vol. 2325, pages 164-179, December 2003.

85. X. Fan, C. S. Ellis, A. R. Lebeck, "Modeling of DRAM Power Control Policies Using Deterministic and Stochastic Petri Nets," in *Proceedings of the Workshop on Power Aware Computing Systems 2002 (PACS '02)*, Springer-Verlag Lecture Notes in Computer Science,vol. 3164, pages 130-140, February 2002.

86. D. Genius, S. Chatterjee, and A. R. Lebeck, "Array Merging: A Technique for Improving Cache and TLB Behavior," in *Workshop on Memory Performance Issues*, in conjunction with International Symposium on Computer Architecture, June 2001.

Poster Presentations & Other Works:

87. S. R. Agrawal, A. R. Lebeck, "Cost-Efficient Cluster Design for High Dimensional Similarity Search," in GPU Technology Conference, March 2015.

88. S. R. Agrawal, V. Pistol, J. Pang, J. Tran, D. Tarjan, A. R. Lebeck, "Rhythm: Harnessing Data Parallel Hardware for Server Workloads," in GPU Technology Conference, March 2014.

89. J. Pang, C. Dwyer, A. R. Lebeck, "mNoC: Large Nanophotonic Network-on-Chip Crossbars with Molecular Scale Devices," General Poster Session at Grace Hopper Celebration, October 2013.

90. S. R. Agrawal, V. Pistol, J. Pang, J. Tran, A. R. Lebeck, "Leveraging GPUs for High Throughput Web Servers," GPU Technology Conference, March 2013.

91. J. Patwardhan, V. Johri, C. Dwyer, A. R. Lebeck, "A Defect Tolerant Self-organizing Nanoscale SIMD Architecture," in Workshop on Edge Computing Using New Commodity Architectures (EDGE), May 2006.

92. C. Dwyer, S. H. Park, T. LaBean, A. R. Lebeck, "The Design and Fabrication of a Fully Addressable 8-tile DNA Lattice," *Proceedings of the Foundations of Nanoscience: Self-Assembled Architectures and Devices* (FNANO), April 2005

93. J. Patwardhan, C. Dwyer, A. R. Lebeck, D. J. Sorin, NANA: A Nanoscale Active Network Architecture, in *Proceedings of the Foundations of Nanoscience: Self-Assembled Architectures and Devices* (FNANO), April 2004.

94. C. Dwyer, V. Johri, M. Cheung, J. P. Patwardhan, A. R. Lebeck, and D. J. Sorin, CAD Support for DNA-Guided Self-Assembly of Nanoelectronics, in *Proceedings of the Foundations of Nanoscience: Self-Assembled Architectures and Devices* (FNANO), April 2004.

95. H Zengh, C. S. Ellis, X. Fan, A. R. Lebeck, A.Vahdat, "ECOSystem: Managing Energy as a First Class Operating System Resource," *ACM International Symposium on Operating Systems Principles (SOSP)*, poster session workshop, October 2001.

In Submission:

1. Ali Razeen, Alvin R. Lebeck, David Liu, Alexander Meijer, Valentin Pistol, Landon P. Cox, "SandTrap: Tracking Information Flows on Demand with Parallel Permissions," submitted to ACM SIGOPS 26th Symposium on Operating Systems (SOSP '17), April 2017.

In Preparation:

1. Xiangyu Zhang, Ramin Bashizade, Chris Dwyer, Alvin R. Lebeck, "Quality Analysis and Optimization of Molecular Optical Gibbs Sampling Units", Proceedings of the International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS), submitted August 2017.

Technical Reports:

1. Yang Liu, Chris Dwyer, Alvin R. Lebeck, Combined Compute and Storage: Configurable Memristor Arrays to Accelerate Search, arXiv:1601.05273, Jan 2016.

1. Jun Pang, Chris Dwyer, Alvin R. Lebeck, "mNoC: Large Nanophotonic Network-on-Chip Crossbars with Molecular Scale Devices," Technical Report CS-2013-02, Department of Computer Science, Duke University, 2013.

2. J. P. Patwardhan, C. Dwyer, A. R. Lebeck, and D. J. Sorin, NANA: A Nano-scale Active Network Architecture, Duke University Computer Science Department Technical Report, 2003.

3. T. Li, A. R. Lebeck, D. J. Sorin, "Spin Detection Hardware for Management of Multithreaded Systems," Duke University Computer Science Department Technical Report, 2004.

4. H. Zeng, C. Ellis, A. Lebeck, A. Vahdat, "Currentcy: Unifying Policies for Resource Management," Duke University Computer Science Technical Report CS-2002-09, May 2002.

5. T. Li, J. Koppanalil, A. R. Lebeck, J. Patwardhan, E. Rotenberg, "A Large, Fast Instruction Window for Tolerating Cache Misses," Duke University Computer Science Technical Report CS-2002-03 March 2002.

6. M. Thottethodi, A. R. Lebeck, S. Mukherjee, "Key Components of High-Performance Routing Algorithms for Virtual Cut-Through Networks," Duke University Computer Science Technical Report CS-2002-02, Jan 2002.

7. H Zengh, C. S. Ellis, X. Fan, A. R. Lebeck, A.Vahdat, "ECOSystem: Managing Energy as a First Class Operating System Resource," Duke University Computer Science Technical Report CS-2001-01, April 2001.

8. M. Thottethodi, A. R. Lebeck, S. Mukherjee, "Self-tuned Congestion Control for Multiprocessor Networks," Duke University Computer Science Technical Report CS-2000-15, November 2000.

9. K. Yocum, D. Anderson, J. Chase, S. Gadde, D. Gallatin, A. R. Lebeck, "Adaptive Message Pipelining for Network Memory and Network Storage," Duke University Computer Science Technical Report CS-1998-10, March 1998.

10. V. P. Pauca, X. Sun, S. Chatterjee, and A. R. Lebeck, "Architecture-Efficient Strassen's Matrix Multiplication: A Case Study of Divide-and-Conquer Algorithms," Duke University Computer Science Technical Report CS-1998-06, May 1998.

11. A. R. Lebeck, D. R. Raymond, and M. S. Thottethodi, "Annotated Memory References: A Mechanism for Informed Cache Management," Duke University Computer Science Technical Report CS-1998-02, February 1998.

12. S. T. Srinivasan and A. R. Lebeck, "Exploiting Load Latency Tolerance in Dynamically Scheduled Processors," Duke University Computer Science Technical Report CS-1998-03, February 1998.

13. J. S. Chase, A. J. Gallatin, A. R. Lebeck, and K. G. Yocum, "Trapeze Messaging API," Duke University Computer Science Technical Report CS-1997-19, November 1997.

14. K. G. Yocum, D. C. Anderson, J. S. Chase S. Gadde, A. J. Gallatin, and A. R. Lebeck, "Balancing Latency and Bandwidth in a High-Speed Network Adapter," Duke University Computer Science Technical Report CS-1997-20, November 1997.

15. M. D. Hill, J. R. Larus, A. R. Lebeck, M. Talluri, D. A. Wood, "Wisconsin Architectural Research Tool Set," *Computer Architecture News*, Vol. 21, No. 4, pages 8-10, August 1993.

16. A. R. Lebeck and D. A. Wood, "Fast-Cache: A New Abstraction for Memory System Simulation," University of Wisconsin Computer Sciences Technical Report #1121, January 1994.

Grants and Contracts:

1. Principle Investigator, Molecular-scale Energy Transport and Computational Phenomena Enabled by DNA Nanotechnology, Office of Naval Research, $2,999,832 total ($1,777,623 10/1/2014 to 9/30/2017, two option years $1,222,209 total). Note: Named PI 08/25/2016.

2. Principle Investigator, CSR:Small: Improving Cloud Services by Exploiting Synchronized Clocks and Software Defined Flash, NSF Computer and Network Systems: Core programs: Computer Systems Research, $506,175, 10/1/2016 to 9/30/2019.

3. Principle Investigator, Intel UPO, parallel computer hardware for research and teaching, equipment (15 Xeon Phis, $7500 estimated value) and $25,000, July 2015.

4. Principle Investigator, NSF REU supplement, $16,000 July 2014.

5. NVIDIA Graduate Fellowship (Sandeep Agrawal), $25,000, 8/1/2014-7/31/2015.

6. Altera University Program DE5 Development Board, $8,000 value February 2014.

7. Principle Investigator, XPS:CLCCA:Collaborative Research: Harnessing Highly Threaded Hardware for Server Workloads, NSF Exploiting Parallelism and Scalability (XPS), $700,000 (Individual portion $350,000) with E. Witchel and M. Silberstein (UT Austin), Sept 2013 – August 2017.

8. Co-Investigator, Stochastic Computing Machines enabled by DNA self-assembly, DARPA MTO DARPA-BAAA-12-64, $2,396,000 (individual portion $546,974) with C. Dwyer (PI: ECE), V. Mansingha (MIT), April 2013 – March 2016.

9. Principle Investigator, nVidia Corp, "Cohort Cores", $25,000 Jan 2013.

10. Principle Investigator, nVidia Corp, "Cohort Cores", $25,000 May 2012.

11. Principle Investigator, NSF REU supplement, $16,000 May 2010. (with C. Dwyer, $8,000 individual portion)

12. Principal Investigator, *nVidia Tesla GPU equipment donation*, value $9000, with J. Pormann (SCSC - OIT), 2009.

13. Co-Investigator, *EMT: MISC: Expanding the Computing Domain with Self-assembled Nanophotonics*, NSF Emerging Models and Technologies, $100,000.00 10/1/2008 to 9/30/2009, with C. Dwyer (PI).

14. Principle Investigator, *Collaborative: Circuit and System Architectures for Self-assembled Nanoscale Computers*, NSF Foundations of Computing Processes and Artifacts, $1,000,000 ($665,456 Duke Portion), 7/15/2007 to 6/30/2011 with C. Dwyer (ECE), K. Chakrabarty (ECE), and S. Washburn (UNC).

15. Principal Investigator, *Integrating FPGA-based Hardware Design into Undergraduate Machine Organization*, Altera Co. 8/31/2006, $57,425.

16. Co-Investigator, *An Evaluation of the Implications of Nanoscale Architectures on Contextual Knowledge Discovery and Memory Systems*, Air Force Research Laboratory—extension of previous grant, 10/1/2005 to 9/31/2007, $498,707 with C. Dwyer (PI).

17. Co-Investigator, *An Evaluation of the Implications of Nanoscale Architectures on Contextual Knowledge Discovery and Memory Systems*, Air Force Research Laboratory, 10/1/2004 to 9/31/2005, $139,179 with C. Dwyer (PI).

18. Principal Investigator, *Nanoarchitecture: Balancing Regularity, Complexity, and Defect Tolerance using DNA for Nanoelectronic Integration*, Duke University Provost's Common Fund, $32,000 with C. Dwyer T. LaBean, J. Liu (Chemistry) and D. Sorin (ECE), 2004.

19. Principal Investigator, *Nanoarchitecture: Balancing Regularity, Complexity, and Defect Tolerance using DNA for Nanoelectronic Integration*, NSF Information Technology Research, CCR-0326157, 9/15/2003 through 9/14/2006, total award $1,200,000 (NCSU subaward $135,000, UNC subaward $135,000) with D. Sorin (ECE), T. LaBean, H. Yan, J. Liu (Chemistry), J. Reif, S. Washburn (UNC), D. Erie (UNC), P. Franzon (NCSU).

20. Principal Investigator, *Architectural Support for Service Level Agreements*, NSF Information Technology Research, CCR-0312561, total $220,000, 08/01/03 - 07/31/06, with D. Sorin (ECE).

21. Principal Investigator, *Nanoarchitecture: Balancing Regularity, Complexity, and Defect Tolerance using DNA for Nanoelectronic Integration*, Duke University Provost's Common Fund, $16,000 with T. LaBean, J. Liu (Chemistry) and D. Sorin (ECE).

22. Principal Investigator, *Communication Oriented Architecture (Pilot Project)*, Intel Corporation, $15,000, with J. Chase and D. Sorin (ECE).

23. Principal Investigator, *Main Memory Power Management*, NSF CCR-0208920 Computer Systems Architecture, total $275,000 (Individual portion $137,500), 08/01/02 - 7/31/05, with C. Ellis.

24. Principal Investigator, *Server Interconnection Networks*, Intel Corporation, $28,000.

25. Co-Investigator, NSF CCR-0204367 Operating Systems and Compilers, *Managing Energy as a First Class Operating System Resource* $250,000 (Individual portion $83,333), 08/01/02 - 7/31/05, with A. Vahdat (PI) and C. Ellis.

26. Principal Investigator, Chia-Lin Yang, Intel Ph.D. Fellowship, $28,800 08/01/00 -7/31/01.

27. Principal Investigator, *Self-tuned Congestion Control for Multiprocessor Interconnection Networks*, $55,918, Compaq Corporation, 01/01/01 - 12/31/01.

28. Principal Investigator, *Load Criticality*, Intel Corporation, $25,000, July 2000.

29. Co-Investigator, *System Support for Energy Management in Mobile and Embedded Workloads* $285,000 NSF Information Technology Research, 09/01/00 - 08/31/02, with Ellis (PI) and Vahdat.

30. Co-Investigator, *System Support for Mobile and Embedded Workloads*, NSF Research Instrumentation Program, NSF EIA-9986024 total award $279,999 ($139,999 NSF and $140,000 Duke matching), 06/ 15/00 through 05/31/03, with Ellis (PI) and Vahdat.

31. Co-Investigator, *Infrastructure for Data-Intensive Computing with Spatial Models*, NSF EIA-9972879 CISE Infrastructure for Experimental Computer Science Research, total award $2,276,571 ($1,550,575 NSF, $725,996 Duke Matching). With Chase (PI), Agarwal, Arge, Edelsbrunner, Ellis, Sun, and Vahdat.

32. Co-Investigator, *Fellowships in Experimental Computer Science*, U. S. Dept. of Education Graduate Assistance in Areas of National Need, 9/1/98 through 8/31/2001, total award $676,377. With C. Ellis, G. Kedem, J. Chase, J. Vitter, L. Arge, M. Littman, O. Astrachan, P. Agarwal.

33. Co-Investigator, *TUNE: Mathematical Models and Transformations for Memory-Friendly Programming*, DARPA/DSO Optimized Portable Application Libraries (OPAL) 2/1/1998 through 1/31/2002, total award $1,899,700 ($1,801,700 DARPA/DSO and $98,000 matching from Duke and UNC). With K. Trivedi (PI, ECE), J. Board (ECE), X. Sun (CS), S. Chatterjee (UNC CS) and P. Hanlon (Michigan Math)

34. Co-Investigator, *TUNE: System Support for Memory Friendly Programming*, NSF Challenges in CISE, NSF-CDA-9726370, 9/15/1997 through 8/31/2000, total award $1,587,929 ($1,547,929 NSF and $40,000 matching from Duke and UNC). With K. Trivedi (PI, ECE), J. Board (ECE), X. Sun (CS), and S. Chatterjee (UNC CS).

35. Principal Investigator, *Informed Caching Environment*, NSF Faculty Early Career Development Program, NSF-MIP-97-02547, 5/1/1997 through 5/1/2001, total award $220,000 ($210,000 NSF and $10,000 matching from Duke Computer Science Department).

36. Co-Investigator, *Intel Technology for Education 2000*, 9/1/1997 through 9/1/2000, total award $1,600,000. With J. Board (ECE), B. Myers (BME), R. Barr (BME), C. Henriquez (BME), S. Smith (BME), G. Trahey (BME), M. Prisant (Chem), B. Muller (Physics), J. Chase (CS), O. Astrachan (CS), X. Sun (CS), and D. Rose (CS).

37. Co-Investigator, *CURIOUS: Center for Undergraduate Education and Research: Integration Through Performance and Visualization*, NSF CISE Education Innovation Program, NSF-CDA-9634475, total award $607,801 ($405,2000 NSF and $202,601 matching from Duke). With O. Astrachan, S. Rodger, P. Agarwal, A. Biermann, G. Kedem, J. Reif, X. Sun, J. Vitter, D. Rose.

Grants and Contracts Submitted in the Previous Three Years:

1. Principle Investigator, SHF:Small:Molecular-Scale Photonic Network on Chip, NSF Computing and Communication Foundations: Core programs: Software Hardware Foundations, $504,333, (Individual portion $492,005) with C. Dwyer, A. Hilton 7/1/2016 to 6/30/2019.

2. Principle Investigator, SHF: Large: Molecular Optical Network-on-Chip (mNoC), NSF Computing and Communication Foundations: Core programs: Software Hardware Foundations, $2,969,997 (Individual portion $749,682) with C. Dwyer, N. Jokerst, M. Brooke, 7/1/2014 to 6/30/2019, Submitted 11/2013.
3. Principle Investigator, IBM Faculty Award, $40,000, submitted 2014.

Invited Talks and Colloquia:

1. *Active Memory: A New Abstraction for Memory System Simulation*, at North Carolina State University, November 11, 1996 host Dr. Tom Conte.
2. *Informed Caching Environment*, at the University of North Carolina—Chapel Hill, April 17, 1998 host Dr. Sid Chatterjee.
3. *Informed Caching Environment*, at Old Dominion University, October 7, 1999 host Dr. Alex Pothen.
4. *Informed Caching Environment*, at North Carolina State University, October 4, 1999 host Dr. Greg Byrd.
5. *Load Latency Tolerance in Dynamically Scheduled Processors*, at Compaq Alpha Development, December 15, 1999 host Dr. Shubhendu Mukherjee.
6. *Informed Caching Environment*, at Intel Corporation Microcomputer Research Laboratory, May 11, 2000 host Dr. Konrad Lai.
7. *Power Aware Page Allocation*, at University of Wisconsin—Madison, September 19, 2000 host Prof. David Wood.
8. *Power Aware Page Allocation*, at University of Michigan—Ann Arbor, September 21, 2000 host Prof. Steven Reinhardt.
9. *Power Aware Page Allocation*, at North Carolina State Univeristy, October 23, 2000 host Prof. Alex Dean.
10. *Power Aware Page Allocation*, at University of Illinois—Champaign-Urbana, October 30, 2000 host Prof. Josep Torellas.
11. *Power Aware Page Allocation*, at University of Texas—Austin, February 30, 2001 host Prof. Doug Burger
12. *Power Aware Page Allocation*, at University of Washington—Seattle, May 22, 2001 host Prof. Susan Eggers.
13. *Power Aware Page Allocation*, at Microsoft Research, May 23, 2001 host Dr. Trishul Chilimbi.
14. *Circuit and System Architecture for DNA-guided Self-assembly of Nanoelectronics,* Air Force Research Laboratory, Rome, NY, July 2004, hosted by Tom Renz.
15. *Circuit and System Architecture for DNA-guided Self-assembly of Nanoelectronics,* IBM TJ Watson Research Center, October 2004, hosted by Michael Gschwind.
16. *Computer Architectures for DNA Self-Assembled Nanoelectronics*, Virginia Nano-computing Workshop, May 2006.
17. *Computer Architectures for DNA Self-Assembled Nanoelectronics*, Air Research Laboratory, Rome NY, June 2006, hosted by Tom Renz.

18. *Energy Management for Secure Mobile Devices*, NSA conference on Secure Mobility, Tampa FL, November 2006, invited by Mark Krawczewicz (conference Chair).
19. *Computer Architectures for DNA Self-Assembled Nanoscale Devices*, Purdue, June 2010, hosted by Mithuna Thottethodi.
20. *Molecular Scale Nanophotonic Networks*, University of Washington, November 2012, hosted by Luis Ceze.
21. *Web Server on a GPU, Not as Crazy as it Sounds*, Facebook, April 2013, hosted by Kaushik Veeraraghavan
22. *Web Server on a GPU, Not as Crazy as it Sounds*, Google, April 2013, hosted by Xiaobo Fan
23. *Web Server on a GPU, Not as Crazy as it Sounds*, NVIDIA, April 2013, hosted by Steve Keckler
24. *The Pursuit of Efficiency in the Many Core Era*, Qualcomm Research, July 2013, hosted by Lisa Hsu
25. *Web Server on a GPU, Not as Crazy as it Sounds*, Oracle Research, March 2014, hosted by Arun Raghavan
26. *Web Server on a GPU, Not as Crazy as it Sounds*, IBM TJ Watson Research Center, April 2014, hosted by Zehra Sura.
27. *Molecular-Scale Nanophotonics for Network-on-Chip and Probabilistic Computing Functional Units*, Oak Ridge National Lab, October 2015, hosted by Jeffery Vetter.
28. *Computing and Biomolecules*, CRA/CCC Architecture 2030, Organizers Luis Ceze and Tom Wenisch, June 2016.

Professional Activities:

1. **Editor**, Computer Architecture Today, the ACM Special Interest Group on Computer Architecture (SIGARCH) online Blog. 2016-present.
2. **Steering Committee:** IEEE Transactions on NanoBioscience.
3. **Associate Editor**, Journal of Instruction-Level Parallelism (2003-2008)
   Guest Editor, ACM Journal on Emerging Technologies for Computing, Special Issue for DAC selected papers, 2007.
4. **Technical Program Co-Chair**, 1st International Conference on Nano-Networks 2006
5. **Program Committees**:
   IEEE/ACM International Symposium on Microarchitecture (MICRO 50) 2017,
   International Symposium on Computer Architecture (ISCA) 2016,
   IEEE Top Picks in Microarchitecture 2015,
   International Conference on Architectural Support for Programming Languages and Operating Systems 2015 (ASPLOS '15)
   International Symposium on Computer Architecture (ISCA) 2014,
   IEEE Top Picks in Microarchitecture 2014,
   International Conference on High-Performance and Embedded Architectures and Compilers 2013 (HiPEAC)) w/ ACM TACO—board of Distinguished Reviewers,
   International Conference on High-Performance and Embedded Architectures and Compilers 2012 (HiPEAC)) w/ ACM TACO—board of Distinguished Reviewers,
   IEEE Top Picks in Microarchitecture 2012,
   International Conference on Architectural Support for Programming Languages and Operating

Systems 2010 (ASPLOS '12)—external committee,
International Conference on High-Performance and Embedded Architectures and Compilers 2012 (HiPEAC)) w/ ACM TACO—board of Distinguished Reviewers,
IEEE International Conference on Green Computing 2011,
International Conference on Architectural Support for Programming Languages and Operating Systems 2010 (ASPLOS '11)—external committee,
IEEE International Symposium on High Performance Computing (HPCA-17) 2011,
IEEE International Conference on Green Computing 2010,
IEEE Top Picks in Microarchitecture 2009,
International Conference on Nano-Networks 2009 (Nanonets '09),
International Conference on Architectural Support for Programming Languages and Operating Systems 2009 (ASPLOS '09),
1st Data Prefetching Championship 2009 (DPC),
International Conference on Nano-Networks 2008 (Nanonets '08),
Computing Frontiers 2008,
IEEE Top Picks in Microarchitecture 2007,
IEEE/ACM International Conference on Nanoscale Architectures 2007 (Nanoarch '07),
International Conference on Nano-Networks 2007 (Nanonets '07),
Computing Frontiers 2007,
Foundations of Nanoscience: Self-Assembled Architectures and Devices 2007 (FNANO '07),
IEEE/ACM International Symposium on Microarchitecture 2006 (MICRO 39),
Foundations of Nanoscience: Self-Assembled Architectures and Devices 2006 (FNANO '06),
International Symposium on Performance Analysis of Systems and Software 2006 (ISPASS '06),
Computing Frontiers 2005 (**Track Chair** on Architectures and Devices for Emerging Nanotechnolgies),
Foundations of Nanoscience: Self-Assembled Architectures and Devices 2005 (FNANO '05),
International Symposium on Performance Analysis of Systems and Software 2005 (ISPASS '05),
Workshop on Duplicating, Deconstructing and Debunking 2003 (with ISCA),
International Symposium on Low Power Electronics and Design 2002 (ISLPED '02),
Workshop on Duplicating, Deconstructing and Debunking 2002 (with ISCA),
Power Aware Computing Systems 2002 (PACS '02),
International Performance and Dependability Symposium 1998.

6. **Invited Panels:**
   Moderator & organizer: 39th International Symposium on Microarchitecture (MICRO) 2006, "Nanotechnology's Role in Shaping Future Architectures",
   Panelist: Fourth International Conference on Formal Methods and Programming Models for Codesign 2006 (MEMOCODE '06),

7. **Speaker**, 1st International Conference on Nano-Networks 2006, ACM International Supercomputing Conference (ICS) May 2000, ACM Sigmetrics Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), May 1995, 22nd International Symposium on Computer Architecture (ISCA), June 1995, Sixth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-VI), October 1994, ASPLOS-IX, October 2000, ASPLOS-XII 2006, ASPLOS 2015, Nano-DDS 2007.

8. **Reviewer**, 20th, 23rd, 25th, 26th, 31st, 32nd, 33rd, 35th, 2010, 2015, 2016 International Symposium on Computer Architecture (ISCA); Sixth, Seventh, Eighth, Tenth, Twelfth, 2016 International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS); 31st, 32nd, 33rd, 34th, 35th, 40th, 44th , 2015, International Symposium on Microarchitecture (MICRO); 2nd Symposium on Operating Systems Design and Implementations (OSDI); Ninth ACM International Conference on Supercomputing (ICS); IEEE Transactions on

Parallel and Distributed Systems (IEEE TPDS), 1992, 1993, 1997, 1998, 2002, 2003; IEEE Transactions on Computers (IEEE TOC) 1996, 1998, 1999, 2000, 2001, 2002, 2003, 2004; Distributed Computing 1995; ACM Transactions on Modeling and Computer Simulation (TOMACS) 1996, 2004; Digital Equipment Corporation Technical Journal 1996; IEEE COMPUTER 1997, 1998; Journal of Parallel and Distributed Computing (JPDC) 1997; ACM Transactions on Computer Systems (TOCS) 1999, 2001, 2008; ACM Transactions on Programming Languages and Systems (TOPLAS) 1997; National Science Foundation (NSF) 1997, 1999, 2002, 2004, 2010; International Symposium on High-Performance Computer Architecture (HPCA) 1997, 2001, 2002, 2003, 2008, 2009,2014; ACM Symposium on Principles and Practice of Parallel Programming (PPoPP) 1997; Proceedings of the IEEE 1997; IEEE Transactions on Embedded Computing (IEEE TEC) 2000; ACM Transactions on Computer Architecture and Optimization (TACO) 2005, 2006, 2009, 2011, 2015; USENIX Technical Program 2006; Journal of Computer Science and Technology (Chinese English Journal) 2006, 2007; Journal of Systems and Software 2006; ACM Symposium on Parallelism in Algorithms and Architectures (SPAA) 2007, ACM Transactions on Parallel Computer (TOPC) 2014.

Wiley&Sons:Textbook 2001, 2006
Elsevier Journal proposal 2009
Various NSF panels
DOE panel and adhoc reviews (2011)
India Dissertation Award, 2014

Software Distributions:

1. **Rhythm**, a framework for using GPUs with server workloads.
2. **Pulse**, an operating system modification that enables dynamic detection of deadlocks in multithreaded programs.
3. **ECOSystem**, a prototype operating system that manages energy as a first class resource, equal to CPU time, memory and other conventional resources.
4. **DNA-CNT**, DNA-Carbon Nanotube Manual Circuit Layout Tool.
5. **DNA-CNT Standard Cells**, Standard cell circuit layouts generated by DNA-CNT and can be used to construct larger circuits.
6. **Trapeze**, a messaging system designed to deliver both low latency and high bandwidth in a gigabit network, has been used as the basis for a messaging system at Digital Equipment Corporation.
7. **Fast-Cache**, a memory system simulation framework. Distributed as part of the Wisconsin Architectural Research Tool Set (WARTS). (pre Duke)
8. **CProf**, a cache profiling system. Distributed as part of the Wisconsin Architectural Research Tool Set (WARTS). WARTS has been licensed by hundreds of sites worldwide. (pre Duke)

Teaching:

1. January 1996 to present - Computer Science Department, Duke University
   COMPSCI 550/ECE 552: Advanced Computer Architecture (formerly CPS 220/ECE252): Fall 2014
   COMPSCI/ECE 250: Computer Architecture (formerly CPS 104): Fall 2013, Spring 2015

COMPSCI 590: Special Topics in Specialized Computer Architectures: Spring 2014, Fall 2015
CPS 104: Computer Organization, Design and Programming, Fall 1998, Spring 2001, Fall 2002, Spring 2003, Spring 2005, Spring 2007, Fall 2007, Spring 2009, Spring 2010, Spring 2011, Fall 2011.
CPS 220: Advanced Computer Architecture I, Fall 1997, Fall 1999, Fall 2001, Fall 2004, Fall 2006, Fall 2008, Fall 2010.
Compsci 650/ ECE 652 (formerly CPS 221): Advanced Computer Architecture II, Spring 1997 (offered as 296), Spring 1998 (with Yousif), Spring 1999 (developed and approved by Duke University as a regular graduate-level course), Spring 2008, Spring 2012, Spring 2016.
CPS 210: Operating System (graduate), Spring 1998 (with Chase and Yousif)
CPS 296: Advanced Topics in Memory Systems, Spring 1996 (developed a one-time offering).
CPS 296: Distributed Sensor Networks, Spring 2002
CPS 300: Graduate Introduction to Computer Science, Fall 2003.
CPS 296: Advanced Topics in Nanocomputers, Spring 2004, Spring 2006 (course development for certificate in Nanoscience).
CPS 296: Parallel Programming, Fall 2009

2. July 2011 - ACACES 2011 Seventh International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems
3. August 1990 to June 1991 - Teaching Assistant, Computer Sciences Dept., University of Wisconsin - Madison.
   Instructor of Introductory Algebraic Programming, Computer Sciences 302. Responsible for lecturing, preparing and grading assignments and exams.

University Service:

1. Chairman, Information Technology Advisory Council (ICAC) 2010-2012,
2. Member, Scholars@Duke Advisory Committee 2010-2012,
3. Lead Coordinator for Computer Systems & Engineering 2011-2013,
4. Chairman, Research Computing Advisory Council (RCAC) 2008-2011,
5. Member, Information Technology Advisory Council (ITAC) 2007-2010,
6. Member ECE reappointment/promotion committee, 2007, 2008, 2010, 2014, 2016
7. Member, Duke Frontiers Program Committee 2004-2005,
8. Member, CSEM Steering Committee (2003-2004),
9. Member, Information Technology Advisory Council (ITAC) 1997-1998,
10. Member, Faculty Search, Department of Electrical and Computer Engineering (ECE) 1997, 2002; active participation in faculty recruiting 2000, 2001, 2005.

Department Service:

1. Chairman Systems Faculty Search 2004, 2005, 2007, 2008, 2009, 2011/2012.
2. Member Communications Committee 2013-2015.
3. Member Department Infrastructure Committee 2011-2012.

4. Chairman Lab Committee 2003-2011.
5. Space Committee 2006-2011.
6. Member strategic planning committee 2009.
7. Chair department reappointment/promotion committee 2008, 2011.
8. Member reappointment/promotion committee 2007, 2008, 2009 (3), 2011.
9. Member graduate curriculum review committee 2007-2009.
10. Undergraduate Committee 2004, 2005, 2010-2012, 2015-present.
11. Chairman Graduate Admissions 2002-2003.
12. Co-Chairman CS/ECE Task Force 2003.
13. Computer Science Electrical and Computer Engineering Liaison Committee 2001-2003.
14. Member Faculty Search, 1996, 1997, 1998, 2000, 2002, 2003.
15. Graduate Admissions 1998, 1999, 2001, 2004, 2013-2015.
16. Undergraduate Major Advisor 2001 to present.

Ph.D. Students:

1. Chia-Lin Yang, Thesis Title: "A Programmable Memory Hierarchy for Prefetching Linked Data Structures," June 2001.
2. Srikanth T. Srinivasan, Thesis Title: "Critical Loads: Characterization, Classification, and Exploitation," July 2001.
3. Mithuna S. Thottethodi, Thesis Title: "Techniques for High Bandwidth, Low Latency Interconnetion Network Operation at High Offered Loads," November 2002 (co-advised with Shubhendu Mukherjee).
4. Xiaobo Fan, Thesis Title: "Power Aware Memory", May 2004 (co-advised with Carla Ellis).
5. Heng Zeng, Thesis Title: "Explicity Energy Resource Management as a First-Class Operating System Resource", May 2004 (co-advised with Carla Ellis).
6. Tong Li, Thesis Title: "Self-monitoring of Thread Interactions for Improved Resource Management in Multithreaded Systems," May 2005 (co-advised with Daniel J. Sorin-ECE).
7. Jaidev Patwardhan, "Architectures for Nanoscale Devices", July 2006.
8. Constatin Pistol, "Structures, Circuits and Architectures for Molecular Scale Integrated Sensing and Computing", May 2009 (co-advised with Chris Dwyer-ECE).
9. Yang Liu, "Architecture for Memristor-based Storage Structures", December 2011.
10. Jun Pang, "Chromophore-Based Nanophotonic Network-on-Chip and Computing Systems," December 2013.
11. Valentin Pistol, "Practical Dynamic Information-Flow Tracking on Mobile Devices," August 2014.
12. Sandeep Agrawal, "Harnessing Data Parallel Hardware for Server Workloads," May 2015.

13. Arjun Rallapali, “Resonance Energy Transfer-Based Molecular Switch Designed Using a Systematic Design Process Based on Monte Carlo Methods and Markov Chains,” August 2016 (co-advised with Chris Dwyer-ECE).
14. Siyang Wang, “A Molecular-scale Programmable Stochastic Process Based On Resonance Energy Transfer Networks: Modeling And Applications,” August 2016 (co-advised with Chris Dwyer-ECE).
15. Craig LaBoda, 2016 expected (co-advised with Chris Dwyer-ECE).
16. Pulkit Misra, 2019 expected.
17. Ramin Bashizade, 2020 expected.
18. Xiangyu Zhang, 2019 expected.
19. Sudharshan Balaji, 2021 expected.

M.S. Students:

1. J. Scot Ransbottom, Thesis Title: “DU-NET: An Implementation of User Level Communication in Digital Unix,” May 1997 (co-advised with Jeff Chase)
2. David Raymond, Thesis Title: “Annotated Memory References: A Mechanism for Informed Cache Management,” May 1998 (Winner Computer Science Department Outstanding Masters Thesis Award)
3. Joseph Fitzgerald, Project Title: “A Study of Multimedia Benchmark Cache Performance,” December 1998
4. Ravin De Souza, Thesis Title: “Visualizing the Memory Behavior of Complex Data Structures,” August 1999
5. Kurt Van Delden, Project Title: “DSRp Implementation and Verification,” May 2000 (co-advised with Amin Vahdat).
6. Brian Hanczaryk, Project Title: “Low Power DRAM Organizations,” May 2002.
7. Vijeta Johri, Thesis Title: “Layout Tools for Nano-scale Circuitry,” May 2004.
8. Jie Xiao, Project Title: "Analysis of Directory-based Coherence Protocol Implementation,” May 2009.
9. Alexander Dutu, Project Title: “Diligent Microprocessors”, May 2012.
10. Ashwin Dandekar (ECE), Project Title: “Porting Rhythm to Intel Xeon Phi,” Dec 2015.
11. Yuxuan Li, Project Title: “Tuning GPU Resources in a Multitenant Environment”, May 2016.

Undergraduate Researchers

1. Kelly Shaw (Summer 1997)
2. Carl Mummert (Summer 1999)
3. Emma Wong (Fall 1999, Spring 2000)
4. Michael Tunick (Fall 2007)

5. Ken Leiter (Spring 2008)
6. Cheney Tsai (CSURF 2010-2011)
7. Michael Zhou (Fall 2011)
8. Helio Liu (Fall 2013)
9. Ellango Jothimurugesan (Spring 2014-2015)
10. Chris Dee (Summer 2014-2016)
11. Xian (Victor) Wang (Spring 2017)
12. Alex Boldt (Spring 2017)

Ph.D. Committees:

Surendar Chandra (advisor Ellis), William Rankin (advisor Board: ECE), Syam Gadde (advisor Chase), Yue Ma (advisor Trivedi), Aristoteli Iordanidis (advisor Kannapolis ECE), Darrell Anderson (advisor Chase), Ken Yocum (advisor Chase), Ron Doyle (advisor Chase), Rajiv Wickremesinghe (advisor Chase), Erin Parker (advisor Chatterjee: UNC), Angela Dalton (advisor Ellis), Rebecca Braynard (advisor Ellis), Justin Moore (advisor Chase), Patrick Reynolds (advisor Vahdat), Albert Meixner (advisor Sorin, ECE), Fred Bower (advisor Sorin, ECE), Anita Lungu (advisor Sorin, ECE), Bogdan Romenscu (advisor Sorin, ECE), Vincent Mao (advisor Dwyer, ECE), Viresh Thusu (advisor Dwyer, ECE), Bing Xie (advisor Chase), Bi Wu (advisor Cox), Botong Huang (advisor Babu), Meng Zengh (advisor Sorin, ECE), Weidan Wu (advisor Lee, ECE), Vishwa Nellore (advisor Dwyer), Mohammad Mottaghi (advisor Dwyer), Songchun Fan (advisor Lee, ECE), Qiuyun Wang (advisor Lee, ECE), Ali Razeen (advisor Cox), Ziqiang (Patrick) Huang (advisor Hilton & Lee, ECE).

M.S. Committees:

Yong Gao, 1996, Nnaemeka Egwuekwe, 1996, Samir Kotia (ECE), 1997, Wei-Chun Chang, 1997, Hau Fung Yung, 1997, Chetan Goyal, (ECE) 1998, Abhijeet Deore, (ECE) 1998, Wendy Wang, 1998, Haifeng Yu, 1999, Rui He, 2000, Wei Li, 2000, Sriram Sellappa, (UNC) 2000, Tao Jin, 2000, John Burchett, (ECE) 2000, Hu Pan, 2000, Prachi Thackar, 2001, Yun Fu, 2001, Sita Iyer 2005, Vincent Mao (ECE) 2007, Shawn Smith (ECE) 2007, Luis Campos (ECE) 2007, Nicole Felice (ECE) 2016.

ECE Quals Committees:

Vishwa Nellore (2011), Siyang Wang (2011), Qiuyun Wang (2013), Craig LaBoda (2015), Shi Jin (2016), Raul Vyas (2016), Ziqiang (Patrick) Huang (2016), Xin Song (2016), Shalin Shah (2016).

Research Interest:

Computer architecture and its intersection with systems and tools, architectures for emerging technologies, memory system design and analysis for both serial and parallel architectures (multicore), and energy efficient computing.

Professional Affiliations:

1. Association for Computing Machinery (ACM).

2. Fellow, Institute of Electrical and Electronic Engineers (IEEE).