Lisa Wu **Wills**

Assistant Professor
of Computer Science and Electrical and Computer Engineering

lisa@cs.duke.com
D304 LSRC · 308 Research Drive · Durham · NC 27701

Research Interests

Computer architecture, domain-specific applications and accelerators, hardware-software co-designs, energy-efficient computing, performance analysis, mapping compute- or memory-intensive applications onto existing and novel architectures, emerging applications related to big data analytics such as graph, database, and genomic analytics, artificial intelligence for computer designs, natural language processing for protein discovery, and interdisciplinary research in fields of computer architecture and healthcare that have a direct impact on improving human lives.

Education

University of California, Berkeley, CA · 2016–2019
Postdoctoral Researcher, Electrical Engineering and Computer Science
Research Sponsor : Professor Krste Asanovic · Research Mentor : Professor David Patterson

Columbia University, New York, NY · May 2014
PhD, Computer Science
Research Advisor : Professor Martha Kim · Dissertation : Accelerating Similarly-Structured Data

University of Michigan, Ann Arbor, MI
Masters of Science, Computer Science and Engineering
Research Advisor : Professor Todd Austin · Master's Thesis : A Fast and Flexible Architecture for Secure Communication

University of Illinois, Urbana-Champaign, IL
Bachelor of Science, Electrical and Computer Engineering

Awards and Honors

- **Selected for Participation at the Dagsuhl Seminar 2024** for Hardware Support for Cloud Database Systems
- **VMWare Early Career Faculty Grant Award 2023**
- **Selected for ISCA 25-Year Retrospective 2023** for Genesis
- **ISPASS Best Paper Award 2023** for PyTFHE
- **IEEE Micro Top Pick Honorable Mention 2023** for SNS
- **Selected for Participation at the Grainger Foundation NAE Frontiers of Engineers US Symposium 2022**
- **IEEE Micro Top Pick 2021** for Genesis
- **National Science Foundation (NSF) Faculty Early Career Development Program (CAREER) Award 2021**
- **Google "Rising" Systems Faculty Award 2020**
- **Facebook Systems for Machine Learning (SysML) Research Award 2020**
- **Clare Boothe Luce Assistant Professorship 2019–2024**
- **IEEE Micro Top Picks Honorable Mention 2017** for Graphicionado
- **MICRO Best Paper Award 2016** for Graphcionado
- **IEEE Micro Top Pick 2015** for Q100
- **ASPLOS Best Paper Nominee 2014** for Q100
- **IEEE Micro Top Pick 2014** for Hardware Accelerated Range Partitioner

Research Experience

Present – July 2019

Assistant Professor of Computer Science and ECE | APEX Lab · Duke University, Durham, NC
Clare Boothe Luce Assistant Professor of Computer Science and ECE
Accelerating Natural Language Processing for Protein Discovery. Leveraging natural language processing to predict protein binding and expedite drug discovery.
Leveraging Artificial Intelligence to Expedite the Designing of Computer Hardware. Using open-source hardware designs to train deep-learning-based AI models to predict the area, power, and timing of hardware designs in the wild ultrafast.
Systolic-array-based Heterogeneous Accelerator Performance Simulator. Fast, accurate, and open-sourced performance simulator to expedite the exploration and evaluation of accelerator architecture and microarchitecture.

Quantitative Evaluation of Accelerator Composer Productivity. Design and implement important acceleratable kernels using the Accelerator Composer and HLS and compare the resultant system performance as well as implementation effort and productivity.
Accelerating Homomorphic Encryption. Expanding the acceleration of Homomorphic Encryption to unexplored application domains such as Transformer-based inference.
Accelerating Genomic Simulation. Accelerating QBiC Pred open source genomic simulation framework using software and hardware techniques.

Summer 2019 – Fall 2016 | **Postdoctoral Researcher | ASPIRE and ADEPT Labs · University of California, Berkeley, CA**
Research sponsor : Professor Krste Asanović
Research mentor : Professor David Patterson
Accelerating Genomics using AWS EC2 F1 Instances. Architected, designed, and deployed a high performing hardware accelerated genomic analytics system on FPGAs in the cloud.
Accelerator Composition Framework for FPGAs in the Cloud.

Fall 2016 – Fall 2014 | **Research Scientist | Intel Labs, Santa Clara, CA**
Accelerator for Graph Analytics. Led a research project to architect and design an efficient reconfigurable, domain-specific hardware accelerator that can process graph analytics workloads with orders of magnitude in efficiency compared to optimized software.
Accelerating Dense and Sparse Matrix Operations using Specialization.

Summer 2014 – Fall 2010 | **Research Assistant | ARCADE Lab · Columbia University, New York, NY**
Database Processing Units (DPUs). Architected and designed a specific instance of a stream-based DPU for efficient processing of analytic database workloads.
Hardware Accelerated Data Partitioner. Architected and designed an efficient hardware accelerated data partitioner that can be used for workloads that exhibit divide-and-conquer or map-reduce computation.
Datatype Acceleration. Architected Abstract Datatype Instructions (ADIs) for hash tables and sparse vectors and showed promising potential for accelerating datatypes.

Publications

2025

- Jian Weng, Boyang Han, Derui Gao, Wanning Zhang, An Zhong, Ceyu Xu, Jihao Xin, Yangzhixin Luo, **Lisa Wu Wills**, and Marco Canini, "Assassyn : A Unified Abstraction for Architectral Simulation and Implementation", to appear at the *International Symposium of Computer Architecture (ISCA) 2025.*
- Christopher Kjellqvist, Brendan Peercy, Alvin R. Lebeck, and **Lisa Wu Wills**, "Beethoven : A Heterogeneous Multi-Core Accelerator System Composer", to appear at the *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2025.* **Upcoming Tutorial at ISCA 2025.**
- Mansi Choudhary, Jiaao Ma, Christ Kjellqvist, and **Lisa Wu Wills**, "COCOSSim : A Cycle-Accurate Simulator for Heterogeneous Systolic Array Architectures", to appear at the *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2025.*
- Christopher Kjellqvist, **Lisa Wu Wills**, and Alvin R. Lebeck, "BigLittleMCA : A Spatially-Optimal Tiled Hardware Accelerator for MCMC Image Processing", to appear at the *ACM Transactions on Architecture and Code Optimization (TACO) 2025.*
- Yannis Chronis, Anastasia Ailamaki, Lawrence Benson, Helena Caminal, Jana Giceva, Dave Patterson, Eric Sedlar, and **Lisa Wu Wills**, "Databases in the Era of Memory-Centric Computing", *Conference on Innovative Data Systems Research (CIDR) 2025.*

2024

- Mansi Choudhary, Ceyu Xu, and **Lisa Wu Wills**, "TPUSim : A Simulator for TPU-like Architectures", *Poster at the IEEE International Symposium for Workload Characterization (IISWC) 2024.*
- Mansi Choudhary, Ceyu Xu, and **Lisa Wu Wills**, "LLaMA Characterization for Future Hardware", *Poster at the IEEE International Symposium for Workload Characterization (IISWC) 2024.*
- Wenji Fang, Yao Lu, Shang Liu, Qijun Zhang, Ceyu Xu, **Lisa Wu Wills**, Hongce Zhang, and Zhiyao Xie, "Transferable Pre-Synthesis PPA Estimation for RTL Designs With Data Augmentation Techniques", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) 2024.*

2023

- Ceyu Xu, Pragya Sharma, Tianshu Wang, and **Lisa Wu Wills**, "Fast, Robust, and Transferable Prediction for Hardware Logic Synthesis". *International Symposium on Microarchitecture (MICRO) 2023.*
- Wenji Jang, Yao Lu, Shang Liu, and Qijun Zhang, Ceyu Xu, **Lisa Wu Wills**, Hongce Zhang, and Zhiyao Xie, "MasterRTL : A Pre-Synthesis PPA Estimation Framework for Any RTL Design". *International Conference on*

Computer-Aided Design (ICCAD) 2023.

- Erika S. Alcorta, Andreas Gerstlauer, Chenhui Deng, Qi Sun, Zhiru Zhang, Ceyu Xu, **Lisa Wu Wills**, Daniela Sanchez Lopera, Wolfgang Ecker, Siddharth Garg, and Jiang Hu, "Special Session : Machine Learning for Embedded System Design". *International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), part of Embedded Systems Week (ESWEEK) 2023.*
- Jiaao Ma, Ceyu Xu, and **Lisa Wu Wills**, "PyTFHE : An End-to-End Compilation and Execution Framework for Fully Homomorphic Encryption Applications". *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2023.* **Best Paper Award.**

2022

- Ceyu Xu, Chris Kjellqvist, and **Lisa Wu Wills**, "SNS's not a Synthesizer : A Deep-Learning-Based Synthesis Predictor". *International Symposium on Computer Architecture (ISCA) 2022.* **IEEE Micro Top Pick Honorable Mention.**
- Isaac S. Robson, Ceyu Xu, and **Lisa Wu Wills**, "ProSE : The Architecture and Design of a Protein Discovery Engine". *ACM Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2022.*
- Phyllis Ang, Bhuwan Dhingra, and **Lisa Wu Wills**, "Characterizing the Efficiency vs Accuracy Trade-off for Long-Context NLP Models". *Workshop on Efficient Benchmarking in NLP (NLP Power !) 2022.*

2021

- Tae Jun Ham, David Bruns-Smith, Brendan Sweeney, Yejin Lee, Seong Hoon Seo, U Gyeong Song, Young H. Oh, Krste Asanovic, Jae W. Lee, and **Lisa Wu Wills**, "Accelerating Genomic Data Analytics with Composable Hardware Acceleration Framework". **IEEE Micro Top Picks***, Volume 41, Issue 3, May-June 2021.*
- Chris Kjellqvist, **Lisa Wu Wills**, and Alvin R. Lebeck, "A Case for Down-Scaled Burn-In for MCMC Accelerators". *IBM-IEEE AI Compute Symposium (AICS) 2021.*

2020

- Tae Jun Ham, David Bruns-Smith, Brendan Sweeney, Yejin Lee, Seong Hoon Seo, U Gyeong Song, Young H. Oh, Krste Asanovic, Jae W. Lee, and **Lisa Wu Wills**, "Genesis : A Hardware Acceleration Framework for Genomic Data Analysis". *International Symposium on Computer Architecture (ISCA) 2020.* **IEEE Micro Top Pick.**

2019 and prior

- **Lisa Wu**, David Bruns-Smith, Frank A. Nothaft, Qijing Huang, Sagar Karandikar, Johnny Le, Andrew Lin, Howard Mao, Brendan Sweeney, Krste Asanović, David A. Patterson, and Anthony D. Joseph, "FPGA Accelerated INDEL Realignment in the Cloud". *IEEE International Symposium on High-Performance Computer Architecture (HPCA) 2019.*
- **Lisa Wu**, Frank A. Nothaft, Brendan Sweeney, David Bruns-Smith, Sagar Karandikar, Johnny Le, Howard Mao, Krste Asanovic, David A. Patterson, and Anthony D. Joseph, "Accelerating Duplicate Marking in the Cloud". *Workshop on Accelerator Architecture in Computational Biology and Bioinformatics (AACBB) 2018.*
- Tae Jun Ham, **Lisa Wu**, Narayanan Sundaram, Nadathur Rajagopalan Satish, and Margaret Martonosi, "Graphicionado : High-Performance and Energy-Efficient Accelerator for Graph Analytics". *International Symposium on Microarchitecture (MICRO) 2016.*
- **Lisa Wu**, Andrea Lottarini, Timothy K. Paine, Martha A. Kim, and Kenneth A. Ross, "The Q100 Database Processing Unit". **IEEE Micro Top Picks***, Volume 35, Issue 3, May-June 2015.*
- **Lisa Wu**, Orestis Polychroniou, Raymond J. Barker, Martha A. Kim, and Kenneth A. Ross, "Energy Analysis of Hardware and Software Range Partitioning". *ACM Transaction on Computer Systems (TOCS), Volume 32, Number 3, September 2014.* **Invited Article**.
- **Lisa Wu**, Raymond J. Barker, Martha A. Kim, and Kenneth A. Ross, "Hardware Partitioning for Big Data Analytics". **IEEE Micro Top Picks***, Volume 34, Issue 3, May-June 2014.*
- **Lisa Wu**, Andrea Lottarini, Timothy K. Paine, Martha A. Kim, and Kenneth A. Ross, "Q100 : The Architecture and Design of a Database Processing Unit". *ACM Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2014.* **Best Paper Nominee. IEEE Micro Top Pick.**
- **Lisa Wu**, Raymond J. Barker, Martha A. Kim, and Kenneth A. Ross, "Navigating Big Data with High-Throughput Energy-Efficient Data Partitioning". *International Symposium on Computer Architecture (ISCA) 2013.* **IEEE Micro Top Pick.**
- **Lisa Wu** and Martha A. Kim, "Acceleration Targets : A Study of Popular Benchmark Suites". *Dark Silicon Workshop (DaSi) 2012, held in conjunction with ISCA 2012.*
- **Lisa Wu**, Martha A. Kim, and Stephen A. Edwards, "Cache Impacts of Datatype Acceleration". *IEEE Computer Architecture Letters (CAL) 2011.*
- Chris Weaver, Rajeev Krishna, **Lisa Wu**, and Todd Austin, "Application Specific Architectures : A Recipe for Fast, Flexible, and Power Efficient Designs". *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES) 2001.*

- **Lisa Wu**, Chris Weaver, and Todd Austin, "Cryptomaniac : A Fast Flexible Architecture for Secure Communication". *International Symposium on Computer Architecture (ISCA) 2001.*

Grants/Research Awards

- "The Design and Fabrication of a Proof of Concept ProSE-based Accelerator for Efficient Transformer-style Model Inference", **Principle Investigator**, Meta Sponsored Research Award, awarded $450K in November 2023 for three years.
- "Athena : AI Institute for Edge Computing Leveraging Next Generation Networks : AI-powered Computer Systems at the Edge", **Senior Investigator**, NSF AI Institute, awarded $555K starting in October 2021 for five years.
- "Applications Driving Architectures (ADA) Research Center : Algorithm-Driven Architectures", **co-Principle Investigator**, a Joint University Microelectronics Program (JUMP) Center funded by a consortium of industrial participatns (SRC) and DARPA, awarded $296K starting in August 2021 for two years.
- "CAREER : Effectuating Hardware-Accelerated Systems with Domain-Specific Primitives", **Principle Investigator**, NSF Faculty Early Career Development Program (CAREER) Award, awarded $544K starting in March 2021 for five years.
- "Accelerating and Deploying Natural Language Processing Systems in Data Centers", **Principal Investigator**, Facebook Research Award on Systems for Machine Learning, awarded $50K in February 2020 for one year.

Patents

- **Lisa K. Wu**, Tae Jun Ham, Nadathur Rajagopalan Satish, and Narayanan Sundaram, "Instructions, Circuits, and Logic for Graph Analytics Acceleration". *United States Patent Application No. 20170286122*; filed Oct 2017.
- Jesus Corbal, Roger Espasa Sans, Milind B. Girkar, **Lisa K. Wu**, Dennis R. Bradford, and Victor W. Lee, "System, Apparatus, and Method for Aligning Registers". *United States Patent Application No. 2012254589*; filed Oct 2012.
- Jesus Corbal, Bret L. Toll, Robert C. Valentine, Jeffrey G. Wiedemeier, Sirdhar Samudrala, Milind B. Girkar, Thomas A. Forsyth, Elmoustapha Ould-Ahmed-Vall, Dennis R. Bradford, and **Lisa K. Wu**, "Systems, Apparatuses, and Methods for Blending Two Source Operands into a Single Destination Using a Writemask". *United States Patent Application No. 20120254588*; filed Oct 2012.
- Jesus Corbal, Andrew T. Forsyth, Thomas D. Fletcher, **Lisa K. Wu**, and Eric Sprangle, "Super multiply add (super MADD) instructions with three scalar terms". *United States Patent No. 9792115*; filed Dec 2011, issued Oct 2017.
- Edward T. Grochowski, Dennis R. Bradford, George Z. Chrysos, Andrew T. Forsyth, Michael D. Upton, and **Lisa K. Wu**, "Apparatus and method for efficient gather and scatter operations". *United States Patent No. 9785436*; filed Sep 2012, issued Oct 2017.
- Robert C. Valentine, Jesus Corbal, Roger Espasa Sans, Robert D. Cavin, Bret L. Toll, Satiago Glalan Duran, Jeffrey G. Wiedemeier, Sridhar Samudrala, Milind B. Girkar, Edward T. Grochowski, Jonathan C. Hall, Dennis R. Bradford, Elmoustapha Ould-Ahmed-Vall, James C. Abel, Mark Charney, Seth Abraham, Suleyman Sair, Thomas A. Forsyth, **Lisa Wu**, and Charles Yount, "Vector friendly instruction format and execution thereof". *United States Patent No. 9513917*; filed Jan 2014, issued Dec 2016.
- Jesus Corbal, Andrew T. Forsyth, **Lisa K. Wu**, and Thomas D. Fletcher, "Instruction and logic to provide vector linear interpolation functionality". *United States Patent No. 9766886*; filed Dec 2011, issued Sep 2017.
- Jesus Corbal, **Lisa K. Wu**, George Z. Chrysos, Andrew T. Forsyth, and Ramacharan Sundararaman, "Prefetch with request for ownership without data". *United States Patent No. 9430389*; filed Dec 2011, issued Aug 2016.

Advising and Mentoring Experience

Graduate Research Advising

- **Ning Liang** (Fall 2024 to present)
  Duke University, CS PhD candidate
  Project : Benchmarking and acccelerating vector database
- **Mansi Choudhary** (Fall 2022 to present)
  Duke University, ECE PhD candidate
  Project : Accelerating LLM, Taping-out an edge Transformer accelerator
- **Pragya Sharma** (Dec 2022 to Nov 2024)
  Duke University, ECE PhD candidate
  Project : Accelerating pose estimation and gesture recognition
- **Jiaao (Mason) Ma** (Fall 2021 to present)
  Duke University, CS PhD candidate
  Project : Accelerating homomorphic encryption
- **Chris Kjellqvist** (Fall 2020 to Present)
  Duke University, CS PhD candidate
  Projects : Accelerator Composer, MCMC accelerators

- **Ceyu (Entropy) Xu** (Summer 2020 to Dec 2024)
  Duke University, CS PhD 2024 · Now : Postdoctoral Fellow at Hong Kong University of Science and Technology
  Projects : Accelerating LLM, AI-based synthesis predictor, Taping-out an edge Transformer accelerator, Accelerating natural language processing for drug discovery
- **Phyllis Ang** (Fall 2019 to Spring 2022)
  Duke University, CS MS 2022 · Now : Performance Architect at NVIDIA
  Projects : Long input sequence benchmark for natural language processing, Accelerator Composer

Postdoc Research Mentoring

- **Tae Jun Ham** (Summer 2019 to Spring 2021)
  Postdoctoral researcher at Seoul National University · Now : Researcher at Google
  Project : Accelerating genomic analytics

Graduate Research Mentoring

- **Eyes Robson** (Fall 2019 to Fall 2022)
  UC Berkeley, CompBio PhD candidate
  Project : Accelerating natural language processing for drug discovery
- **Nathan Pemberton** (Fall 2020)
  UC Berkeley, CS PhD candidate advised by Randy Katz
  Project : Firemarshall
- **Tae Jun Ham** (Summer and Fall 2015)
  Princeton University, EE PhD 2018 advised by Margaret Martonosi
  Project : Accelerating graph analytics (intern at Intel Labs)
- **David Bruns-Smith** (Fall 2017 to Fall 2019)
  UC Berkeley, EECS PhD candidate advised by Krste Asanović
  Projects : Accelerating genomic analytics, Accelerator Composer, Accelerating Bayesian inference
- **Eric Love** (Fall 2014 to Fall 2016, Spring 2019)
  UC Berkeley, EECS PhD candidate advised by Krste Asanović
  Master's Thesis : Ressort – An Auto-Tuning Framework for Parallel Shuffle Kernels
  Project : Autotuning for database query executions
- **Andrea Pellegrini** (Summer 2011)
  University of Michigan Ann Arbor, EECS PhD 2013 advised by Valeria Bertacco · Now : Computer engineer at ARM
  Project : Path-finding for Many Integrated Cores architecture (intern at Intel Xeon Phi product dev team)
- **Eric Hill** (Summer 2005)
  University of Wisconsin Madison, EE PhD 2008 advised by Mikko Lipasti · Now : Computer architect at Intel
  Project : Performance validation for Xeon servers (intern at Intel Xeon Server product development team)

Undergraduate Research Mentoring

- **Patrick Hardison** (Spring 2025 to Present)
  Duke University, ECE BS expected 2025
  Project : Accelerator Composer
- **Tianshu Wang** (Fall 2022 to Fall 2023)
  Duke University, ECE BS 2023, MS 2024 · Now : Tesla hardware engineer; joining Stanford as an ECE PhD candidate 2025
  Project : AI-based synthesis predictor
- **Brendan Peercy** (Fall 2022 to Spring 2024)
  Duke University, ECE BS 2024, MS 2025
  Project : Accelerator Composer
- **Sarah Lim** (Spring 2020 to Fall 2020)
  Duke University, ECE BS 2021
  Project : Accelerator Composer
- **Brendan Sweeney** (Fall 2017 to Spring 2020)
  UC Berkeley, EECS BS 2020 · Now : ECE PhD cadidate at UT Austin advised by Mattan Erez
  Projects : Accelerating genomic analytics, Accelerator Composer
- **Brandon Guo** (Spring 2020)
  Duke University, ECE BS 2020 · Now : Azure engineer at Microsoft
  Project : Accelerator Composer
- **Jonny Le** (Spring 2017 to Fall 2017)
  UC Berkeley. EECS MS 2018
  Project : Accelerating genomic analytics
- **Andrew Lin**
  UC Berkeley, EECS BS 2017 · Now : CPU performance architect at Apple
  Project : Accelerating genomic analytics
- **Timothy Paine**
  Columbia University, Computer Engineering MS 2015 · Now : Athena core developer at J.P. Morgan
  Project : Accelerating database analytics

Teaching Experience

Instructor/Lecturer

- Duke University
  CS/ECE 590/557 Computer Architecture and Hardware Acceleration · Spring 2025, Spring 2023, Spring 2021, Fall 2019
  This course is a graduate-level seminar in computer architecture with special topics in hardware acceleration. This course surveys the landscape of hardware acceleration from historical contexts to recent trends in system designs spanning a variety of application domains. This course also covers the taxonomy of accelerators, the hardware-software co-designing of accelerators, and the deployment of accelerators using the AWS cloud.
- Duke University
  CS 550/ECE 552 Advanced Computer Architecture I · Fall 2024, Fall 2022
  The objective of this course is to learn the fundamental aspects of computer architecture design and analysis. Topics include processor design, pipelining, superscalar, out-of-order execution, caches (memory hierarchies), virtual memory, storage systems, simulation techniques, parallel architectures, warehouse scale computing, domain-specific accelerators, and technology trends and future challenges.
- Duke University
  CS/ECE 210 Introduction to Computer Systems · Spring 2024, Spring 2022
  This course provides a programmer's view of how computer systems execute programs and store information. It examines key computational abstraction levels below modern high-level languages; introduction to C, number and data representations, computer memory, assembly language, memory management, the operating-system process model, high-level machine architecture including the memory hierarchy, and introduction to concurrency.
- Duke University
  CS/ECE 250 Undergraduate Computer Architecture · Fall 2020
  This is an introductory undergraduate-level course in computer architecture. To gain a basic understanding of a computer system, students will learn a wide variety of topics including C programming language, RISC-V assembly language, computer arithmetic, basic logic design, basic control and datapath design, pipelining, caches and memory hierarchy, parallelism, and warehouse scale computing.
- University of California Berkeley
  CS 252 Graduate Computer Architecture · Spring 2017
  This course is an introductory graduate-level course in computer architecture. This course provides the essential background for students intending to pursue research in computer architecture and related fields. This course also serves as preparation for the UC Berkeley EECS computer architecture oral prelim examination.

Talks

Conference Talks

- Synthesis Prediction : Use Deep Learning to Expedite the Hardware Architecture and Design Process · Fall 2023 · **Invited Special Session Speaker**
  Embedded Systems Week (ESWEEK) Special Session : Machine Learning for Embedded System Design
- Balancing Flexibility with Specificity : How to Accelerate Genomic Analytics with a Composable Framework · Summer 2022 · **Invited Keynote Speaker**
  ISCA Workshop on Accelerator Architecture in Computational Biology and Bioinformatics (AACBB)
- The Road Less Traveled and The Lessons Learned Along the Way · Spring 2022 · **Invited Keynote Speaker**
  Young Architect Workshop (YArch) co-located with ASPLOS
- Industry vs. Academia Research Positions · Spring 2021 · **Invited Speaker**
  Computing Research Association-Widening Participation (CRA-WP) Grad Cohort for Women
- Accelerators · Summer 2020 · **Invited Speaker/Panelist**
  International Symposium on Computer Architecture (ISCA) Mini-Panel
- FPGA Accelerated INDEL Realignment in the Cloud · Spring 2019
  International Symposium on High-Performance Computer Architecture (HPCA)
- Unexpected yet Common : Industry after PhD · Fall 2018 · **Invited Speaker/Panelist**
  Grace Hopper Celebration (GHC) Career Panel
- Accelerating Duplicate Marking in the Cloud · Spring 2018
  Workshop on Accelerator Architecture in Computational Biology and Bioinformatics (AACBB)
- The Road Less Traveled? · Fall 2017 · **Invited Speaker**
  MICRO Workshop on Career for Women and Minorities in Computer Architecture
- Q100 : The Architecture and Design of a Database Processing Unit · Spring 2014
  ACM Architectural Support for Programming Languages and Operation Systems (ASPLOS)
- Navigating Big Data with High-Throughput Energy-Efficient Data Partitioning · Summer 2013
  International Symposium on Computer Architecture (ISCA)
- Acceleration Targets : A Study of Popular Benchmark Suites · Summer 2013
  ISCA Workshop on Dark Silicon (DaSi)
- Cache Impacts of Datatype Acceleration · Fall 2011

HPCA Special Session for Best of IEEE Computer Architecture Letters (CAL)
- Cryptomaniac : A Fast Flexible Architecture for Secure Communication · Summer 2001
  International Symposium on Computer Architecture (ISCA)

Invited Industry Talks
- Broadening the Field of Heterogeneous Computing
  Meta Platforms Inc., Bellevue, WA · Fall 2024
- Leveraging AI to Expediate Hardware Design
  Google Invited Workshop on Accelerators, Compute, Reliability, and Security · Summer 2022
- Hardware Acceleration
  IBM Virtual Workshop · Fall 2020
- Research Vision on Computer Architecture and Healthcare
  Google "Rising" Systems Faculty Award Virtual Celebration · Fall 2020
- Hardware Acceleration in the World of Emerging Applications
  IBM T.J. Waston Research, Yorktown Heights, NY · Fall 2019
  Facebook, Boston, MA · Summer 2019
  Microsoft Research, Redmond, WA · Summer 2019
  Google, Mountain View, CA · Summer 2019
  Xilinx, San Jose, CA · Summer 2019
- Stories, not Words : How to Design Efficient Accelerators
  Qualcomm Research, San Diego, CA · Fall 2018
- RISC-V : Free and Open Instruction Set Architecture
  Microsoft Research, Redmond, WA · Fall 2016
- Q100 : The Architecture and Design of a Database Processing Unit
  Intel Labs, Santa Clara, CA · Summer 2014
  NVIDIA Research, Santa Clara, CA · Summer 2014

Services

Conference Program Committee
- International Symposium on Computer Architecture (ISCA) 2025 2024 2023 2022 2021 2017 2016
- Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2025 2024 2022 2021
- International Symposium on Microarchitecture (MICRO) 2024 2023 2022 2021 2019 2017
- International Symposium on High-Performance Computer Architecture (HPCA) 2023 2022 2019
- International Symposium on High-Performance Computer Architecture (HPCA) Industry Session 2021 2016
- International Symposium on Workload Characterization (IISWC) 2024 2023 2022 2020 2019 2015
- International Conference on Parallel Architectures and Compilation Techniques (PACT) 2020
- International Symposium on Code Generation and Optimization (CGO) 2020 2017
- International Symposium on Performance Analysis of Systems and Software (ISPASS) 2017

Conference External Review Committee
- International Symposium on Computer Architecture (ISCA) 2020 2019 2015
- International Symposium on High-Performance Computer Architecture (HPCA) 2025 2020 2019
- International Symposium on Microarchitecture (MICRO) 2015

Conference Organizing Committee
- Program Committee Co-Chair : International Symposium on Workload Characterization (IISWC) 2024
- Sponsorship Co-Chair : International Symposium on Workload Characterization (IISWC) 2023
- Workshops/Tutorials Co-Chair : International Symposium on Microarchitecture (MICRO) 2021
- Industry Liaison Chair : International Symposium on Workload Characterization (IISWC) 2017
- Publicity Chair : International Symposium on Computer Architecture (ISCA) 2015

Workshop Program Committee
- ACM Student Research Competition (SRC) held in conjunction with MICRO 2023
- International Workshop on Benchmarking Machine Learning Workloads on Emerging Hardware (CHALLENGE20) held in conjunction with MLSys 2020
- International Workshop on Accelerating Analytics and Data Management Systems Using Modern Processor and Storage Architectures (ADMS) held in conjunction with VLDB 2020

Journal Selection Committee
- IEEE Micro Top Picks 2023 2021 2020

Journal Editorial Board
- Guest Editor : IEEE Transaction on Computers Special Issue on Domain-Specific Architectures for Emerging Applications 2020

Journal Reviewer

- ACM Transactions on Architecture and Code Optimization (TACO) · April 2021 · January 2020
- IEEE Transactions on Knowledge and Data Engineering (TKDE) · January 2020
- IEEE Micro · August 2019 · December 2017 · June and August 2016

Outreach

- Organizer/Sponsor : First Annual East Coast Chisel Bootcamp 2019

Book Reviewer

- Morgan & Claypool series on Computer Architecture : Compiling Algorithms for Heterogeneous Systems · September 2017

University Services

- ECE Computer Engineering Faculty Search Committee
- Faculty Advisor for ACM-W Duke Chapter
  ACM-W celebrates, informs, and supports women in computing. The Duke ACM-W chapter serves Duke CS/ECE female graduate students at Duke University. It celebrates women in the field of computing and advocates and supports them in their studies, research, and life so they can strive for excellence.
- ECE Undergraduate Studies Committee
  ECE Departmental Committee that governs all affairs related to undergraduate curriculum in ECE.

Work Experience

Xeon Phi Core Architect and Performance Architect | Intel Corporation

- Knights Hill application characterization and analyses of stencil and cloud workloads.
- Knights Corner and Larrabee Vector Processing Unit (VPU) lead architect.

Xeon Performance Architect and Uncore Architect | Intel Corporation

- Quantitative analysis of Xeon system performance.
- Xeon QPI home agent architect.

Itanium Core Microarchitect and Performance Architect | Intel Corporation

- Itanium Instruction Fetch Unit (IBox) microarchitect.
- Performance modeling and projection of Itanium processor cores.

Graduate Rotation Engineer | Inte Corporation

- Performance correlation and functional validation of Xeon multimedia instructions.
- Application optimization for Xeon architectures.

Performance Intern | Apple, Inc.

- Quantitative analysis of Mac system performance.

Network Intern | Hewlett-Packard Company

- WAN test lab development for business network solution services.

Product Intern | Advanced Micro Devices, Inc.

- Post-silicon debug and characterization using Teradyne testers.

References

Available Upon Request